REMARKS

Claims 1-18 are currently pending in the present patent application.

In the subject Office Action, claims 12-17 were rejected under 35 U.S.C. 103(a) as being unpatentable over Ninomiya (U.S. Patent No. 5,809,330) in view of Nakashima (U.S. Patent No. 6,029,211) since the Examiner stated that as per claim 12, Ninomiya teaches a method for determining the function of a circuit board in an enclosure comprising the steps of: displaying an identifying characteristic of the slot inside of the enclosure; detecting the circuit board, and directing the circuit board to perform the function associated of the slot.

The Examiner continued that Ninomiya does not teach a characteristic of a binary representation that allows for a multifunction circuit that associates the particular function based on the detected binary characteristic, but that Nakashima teaches a method in which a characteristic is identified in a binary representation for directing a multifunction circuit board to perform a particular function associated with the detected characteristic; detecting the displayed characteristic on the circuit board; interpreting the detected characteristic on the circuit board; and directing the circuit board to perform the function associated with the interpreted characteristic of the slot. The Examiner concluded that it would have been obvious to one of ordinary skill in the art at the time of the applicants' invention to modify the teachings of Ninomiya with that of Nakashima, and that one of ordinary skill would make such modification in order to reduce overhead of driver installation of functions not being utilized by the PC.

Applicants respectfully disagree with the Examiner concerning the rejection of claim 12 as being unpatentable over Ninomiya in view of Nakashima. Turning now to Ninomiya, Col. 7, lines 46-56, state: "The expansion unit 2 contains a connector **27**, expansion slots including expansion connectors **28** and **29**, as well as **photosensors 30 and 31 to determine the presence of a card**. The connector **27** has a configuration and pin placement scheme enabling it to connect to the expansion connector **26**. Various types of expansion devices are detachably connected to each of a number of expansion units **28** and **29** belonging to the expansion unit 2. Expansion devices include modem cards,

sound cards, graphics adapter cards, SCSI interface cards, multiple I/O cards and other types of ISA Option cards, as well as PCMCIA-type IC cards." (Emphasis added by applicants.). Column 8, lines 4-19, of Ninomiya state: "The **photosensor 30 is a card detection device that detects whether option card 32 is connected to the expansion connector 28, and is located in the card insertion path of the expansion slot**. As shown in the drawing, the photosensor **30** has two protrusions, one side of which is equipped with a photoemitter and the other side of which, facing the first, is equipped with a photoreceptor. When an option card **32** is connected to the expansion connector **28**, the passage of light in the space between these two protrusions, that is, **the space between the photoemitter and the photoreceptor is obstructed by the insertion of the option card 32. In this event the photosensor 30 generates a card detection signal DTE1 indicating that the option card 32 was inserted in the expansion slot**. The card detection signal DTE1 is sent to the system controller **12** via the connectors **27** and **26**, and a flag indicating the insertion of a card is thereupon set in a prescribed status register in the system controller **12**." (Emphasis added by applicants.). Additionally, Col. 8, lines 27-41 of Ninomiya states: "**Card detection devices employing photosensors (light permeable type or reflective type) as shown in this embodiment** are most desirable from the standpoint of accuracy of detection, in terms of such points as reliability, durability and efficiency of space utilization, but card insertion may also be detected by means of a microswitch, for example, or through detection of a change in voltage to certain pins of the expansion connector. The option cards **32** and **33** have address decoders that receive and decode the I/O addresses supplied from the system, determine whether these I/O addresses are the I/O addresses they requested, and said cards operate when it is determined that these I/O addresses are the I/O addresses they requested." (Emphasis added by applicants.).

Ninomiya clearly teaches that the photosensors are simply used for determining whether a card has been inserted into a slot.

Column 6, lines 31-58 of Nakashima state: "By means of the switchable setting of CIS switch setting element 11, personal computer 3 begins to read in, starting from the basic attribute information of the selectively designated CIS. When that information has been completely read, personal computer 3 proceeds to functional attribute information that follows, and reads the data that indicates the completion of that functional attribute information, thereby completing read-in of the data for the selectively designated CIS. With the read-in of the data for this selectively designated CIS, personal computer 3 establishes an environment that enables utilization of the function related to that CIS. Thus in accordance with this embodiment of the present invention, since a plurality of CISs are installed in PC card 1, and each CIS has basic attribute information and functional attribute information, each CIS takes the configuration of a CIS in one single-type or multi-type PC card according to prior art. Thus **the card attribute information (CIS) for a plurality of single-type or multi-type PC cards can be provided for each CIS independently on a single PC card 1**. Accordingly, by assigning a CIS having basic attribute information and functional attribute information to a PC card 1 according to this embodiment of the present invention, it is possible, using PC card 1 according to the present invention, to selectively carry out the operations of a single function, even if personal computer 3 is not provided with a driver having multifunction capability." (Emphasis added by applicants.).

Nakashima clearly teaches that card attribute information (CIS) for a plurality of single-type or multi-type PC cards can be provided for each CIS independently on a single PC card. Nakashima does not teach the identification and deployment of functionality of a PC card as being determined by the slot in which the card is inserted.

Subject claim 12 recites: "A method for determining the function of a multifunction circuit board disposed in a slot in an enclosure, comprising the steps of: **displaying an identifying characteristic of the slot** in a binary representation inside of the enclosure; **detecting the binary representation of the displayed characteristic on the multifunction circuit board**; **interpreting**

the binary representation of **the detected characteristic** on the multifunction circuit board; and directing the circuit board to perform that particular function of the multifunction circuit board associated with the interpreted characteristic of the slot." (Emphasis added by applicants.).

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). Clearly, the step of displaying an identifying characteristic of the slot, the step of detecting the binary representation of the displayed characteristic on the multifunction circuit board, and the step of interpreting the binary representation of the detected characteristic are not taught or suggested by the combination of Ninomiya and Nakashima as suggested by the Examiner.

Claims 13-17 were also rejected under 35 U.S.C. 103(a) as being unpatentable over Ninomiya in view of Nakashima. If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). For the reasons set forth hereinabove, applicants believe that independent claim 12 is patentable over the combination of Ninomiya and Nakashima. Therefore, dependent claims 13-17 are patentable.

Claims 1-10 were rejected under 35 U.S.C. 103(a) as being unpatentable over Ninomiya in view of Nakashima and further in view of Lee (U.S. Patent Number 5,748,912) since the Examiner stated that as per claim 1, Ninomiya teaches an apparatus for determining the function of a circuit board disposed in a slot in an enclosure and in electrical communication with said enclosure, which comprises in combination: (a) means located within said enclosure for displaying an identifying characteristic of the slot; (b) means disposed on said circuit board for detecting the characteristic; and (c) a processor for interpreting the detected characteristic and for directing said circuit board to perform the function associated therewith. The Examiner continued that Ninomiya does not teach a

characteristic of a binary representation that allows for a multifunction circuit that associates the particular function based on the detected binary characteristic, but that Nakashima teaches a method in which a characteristic is identified in a binary representation for directing a multifunction circuit board to perform a particular function associated with the detected characteristic. The Examiner concluded that it would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the teachings of Ninomiya with that of Nakashima, and that one of ordinary skill would make such modification in order to reduce overhead of driver installation of functions not being utilized by the PC.

The Examiner continued that Ninomiya/Nakashima does not disclose a processor disposed on said circuit board, but that Lee analogously teaches an option card with a processor disposed on said circuit board. The Examiner concluded that it would have been obvious to one of ordinary skill in the art at the time of the applicants' invention to insert the option card of Lee into the option card slot of Ninomiya/Nakashima, and that one of ordinary skill in the art would be motivated to make such modifications in order to allow for an efficient and flexible means for users to replace a processor in a unit without exorbitant costs.

Applicants respectfully disagree with the Examiner concerning the rejection of claims 1-10 under 35 U.S.C. 103(a) as being unpatentable over Ninomiya in view of Nakashima and further in view of Lee.

Subject claim 1, recites: "An apparatus for determining the function of a multifunction circuit board disposed in a slot in an enclosure and in electrical communication with said enclosure, which comprises in combination: (a) **means located within said enclosure for displaying an identifying characteristic of the slot** in a binary representation; (b) **means disposed on said multifunction circuit board for detecting** the binary representation of **the characteristic**; and (c) **a processor** disposed on said circuit board for interpreting the detected binary representation of the characteristic and **for directing said multifunction circuit board to perform that particular function** of said multifunction circuit board **associated with the detected characteristic**." (Emphasis added by applicants.).

As stated hereinabove, in order to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). Clearly, means located within said enclosure for displaying an identifying characteristic of the slot; means disposed on said multifunction circuit board for detecting the characteristic; and a processor disposed on said circuit board for interpreting the detected characteristic and for directing the multifunction circuit board to perform that particular function associated with the detected characteristic, are not taught or suggested by the combination of Ninomiya, Nakashima and Lee as suggested by the Examiner.

If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). For the reasons set forth hereinabove, applicants believe that independent claim 1 is patentable over the combination of Ninomiya, Nakashima and Lee. Therefore, dependent claims 2-11 are patentable.

Claims 11 and 18 were rejected under 35 U.S.C. 103(a) as being unpatentable over Ninomiya in view of Nakashima, further in view of Lee, and further in view of Pope et al. (U.S. Patent No. 4,781,066) since the Examiner asserted that Ninomiya/Nakashima modified by the teachings of Lee as applied in claim 1 above as per claims 11 and 18, fails to teach an apparatus wherein said means disposed on said circuit board for detecting the characteristic of the slot comprises a Hall-effect apparatus, while Pope et al. analogously teaches an apparatus wherein said means disposed on said circuit board for detecting the characteristic of the slot comprises a Hall-effect apparatus. The Examiner concluded that it would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Ninomiya and Lee with the above teachings of Pope et al, and that one of ordinary skill would have been motivated to make such modification in order to have a detection system that permits enhanced sensitivity and noise immunity in the system.

Applicants respectfully disagree with the rejection of claims 11 and 18 under 35 U.S.C. 103(a) as being unpatentable over Ninomiya in view of Nakashima, further in view of Lee, and further in view of Pope et al. As stated hereinabove, applicants believe that the combination of Ninomiya and Nakashima does not teach key elements of independent claims 1 and 12, and that Lee does not cure this deficiency. Applicants further believe that the addition of the Pope et al. reference also does not cure this deficiency. Since all claim limitations must be taught or suggested by the prior art in order to establish *prima facie* obviousness of a claimed invention, applicants respectfully believe that the Examiner has not made a proper *prima facie* case for obviousness.

In view of the discussion presented hereinabove, applicants respectfully believe that the Examiner has not made a proper *prima facie* case for obviousness as is required in a rejection under 35 U.S.C. 103(a). Applicants therefore believe that subject claims 1-18 are in condition for allowance, or appeal, the former action by the Examiner at an early date being earnestly solicited.

Reexamination and reconsideration are respectfully requested.

Respectfully submitted,

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